What is claimed is:

1. A semiconductor memory device including a word line, a bit line and a plate line; a sense amplifier and a precharge circuit connected to the bit line; a plate line driving portion having a control transistor that has a control electrode and a main current path and is connected to a plate line; a selection transistor that has a control electrode and first and second main current path ends disposed at both ends of the main current path, the control electrode being connected to the word line and the first main current path end being connected to the bit line; a ferroelectric capacitor that has first and second electrodes, the first electrode being connected to the second main current path end and the second electrode being connected to the plate line; a first power supply that is connected to the sense amplifier and the precharge circuit; a second power supply that is connected to the plate line driving portion, disposed in a separate system from the first power supply and is insulated from the first power supply at the time of non-operation; a first ground line that is connected to the sense amplifier and the precharge circuit; and a second ground line that is connected to the plate line driving portion and insulated from the first ground line:

wherein the semiconductor memory device includes a first semiconductor region where a main current path of the selection transistor is formed; and a second semiconductor region where

a main current path of the control transistor is formed and that is insulated through an insulating film from the first semiconductor region.

2. A semiconductor memory device as set forth in claim 1:

wherein the selection transistor and the control transistor are formed on an SOI substrate, an SOS substrate, or a glass substrate.

3. A semiconductor memory device as set forth in claim 1:

wherein the selection transistor is formed directly on a supporting substrate of an SOI substrate; and

the control transistor is formed through the supporting substrate of the SOI substrate and a first insulating film on a semiconductor film.

4. A semiconductor memory device as set forth in claim 1:

wherein the selection transistor is formed through a supporting substrate of an SOI substrate and a first insulating film on a semiconductor film; and

the control transistor is formed directly on the supporting substrate of the SOI substrate.

5. A semiconductor memory device as set forth in claim 1:

wherein the first semiconductor region and the second

semiconductor region are formed on first and second semiconductor substrates formed in separate bodies;

wherein the first semiconductor substrate and the second semiconductor substrate are disposed with a predetermined separation; and a plate line on the first semiconductor substrate and a control transistor on the second semiconductor substrate are electrically connected with a wiring.

6. A semiconductor memory device as set forth in claim 1:

wherein a transistor that constitutes the sense amplifier and the precharge circuit is formed in the first semiconductor region.

7. A method of fabricating a semiconductor memory device that has a selection transistor and a ferroelectric capacitor including:

forming, on a substrate, first and second semiconductor regions insulated from each other through an insulating film;

forming a selection transistor in the first semiconductor region and a control transistor of a plate line driving portion in the second semiconductor region;

forming, on the selection transistor and the control transistor, through a first insulating film, a ferroelectric capacitor; and

forming a bit line and a plate line through a second insulating film on the ferroelectric capacitor, electrically

connecting the selection transistor to the bit line and the ferroelectric capacitor, and electrically connecting the ferroelectric capacitor and the plate line.

8. A method of fabricating a semiconductor memory device as set forth in Claim 7:

wherein the forming the first and second semiconductor regions includes partially removing a semiconductor film and an insulating film and exposing a supporting substrate in an SOI substrate where the semiconductor film is formed through the first insulating film on the supporting substrate;

wherein the selection transistor is directly formed on the supporting substrate and the control transistor is formed on the semiconductor film.

9. A method of fabricating a semiconductor memory device as set forth in Claim 7:

wherein the forming the first and second semiconductor regions includes partially removing a semiconductor film and an insulating film and exposing a supporting substrate in an SOI substrate where the semiconductor film is formed through the first insulating film on the supporting substrate;

wherein the selection transistor is formed in the semiconductor film, and the control transistor is directly formed on the supporting substrate.

10. A method of fabricating a semiconductor memory device that has a selection transistor and a ferroelectric capacitor

including:

preparing first and second semiconductor substrates;

forming a selection transistor on the first semiconductor substrate and forming a ferroelectric capacitor through a first insulating film on the selection transistor;

forming, on the ferroelectric capacitor, a bit line and a plate line through a second insulating film, electrically connecting the selection transistor to the bit line and the ferroelectric capacitor, and electrically connecting the ferroelectric capacitor to the plate line;

forming, on the second semiconductor substrate, a control transistor of a plate line driving portion; and

electrically connecting the control transistor and the plate line.